WHAT IS CLAIMED IS:

1. A liquid crystal display device comprising:

a thin film transistor within a pixel region defined by a plurality of gate lines and data lines; and

a buffer layer interposed between a gate electrode and source and drain electrodes of the thin film transistor, the source and drain electrodes having a low resistance material.

2. The device as claimed in claim 1, wherein the buffer layer includes a metal.

3. The device as claimed in claim 1, wherein the buffer layer includes titanium (Ti).

4. The device as claimed in claim 1, wherein the gate electrode includes a low resistance material.

5. The device as claimed in claim 4, wherein the low resistance material includes one of aluminum (Al), copper (Cu), and silver (Ag).

6. The device as claimed in claim 1, wherein the low resistance material includes one of aluminum (Al), copper (Cu), and silver (Ag).

7. An in-plane switching mode liquid crystal display (LCD) device comprising:

a thin film transistor having a source electrode, a drain electrode, and a gate electrode within a pixel region defined by a plurality of gate lines and data lines, the source and drain electrodes having a low resistance material;

an ohmic contact layer on the active region; and

a buffer layer on the ohmic contact layer;

wherein the source and drain electrodes are on the buffer layer.

8. The in-plane switching mode LCD device as claimed in claim 7, wherein the gate electrode includes a low resistance material.

9. The in-plane switching mode LCD device as claimed in claim 8, wherein the low resistance material includes one of aluminum (Al), copper (Cu), and silver (Ag).

10. The in-plane switching mode LCD device as claimed in claim 7, wherein the low resistance material includes one of aluminum (Al), copper (Cu) and silver (Ag).

11. The in-plane switching mode LCD device as claimed in claim 7, wherein the buffer layer includes a metal.

12. The in-plane switching mode LCD device as claimed in claim 7, wherein the buffer layer includes titanium (Ti).

13. The in-plane switching mode LCD device as claimed in claim 7, further comprising a gate insulating film on an entire surface including the gate electrode.

14. The in-plane switching mode LCD device as claimed in claim 13, wherein the gate insulating film includes one of silicon nitride film and silicon oxide film.

15. The in-plane switching mode LCD device as claimed in claim 7, further comprising a pixel electrode electrically connected with the buffer layer.

16. The in-plane switching mode LCD device as claimed in claim 15, wherein the pixel electrode includes transparent conductive material.

17. The in-plane switching mode LCD device as claimed in claim 16, wherein the transparent conductive material includes indium tin oxide.

18. An in-plane switching mode liquid crystal display (LCD) device comprising:

a gate electrode on a substrate;

a gate insulating film on an entire surface of the substrate;

a semiconductor layer and an ohmic contact layer on the gate insulating film;

a buffer layer on the ohmic contact layer;

a pixel electrode on the buffer layer;

source and drain electrodes connected with the pixel electrode on the buffer layer;

a passivation layer on the pixel electrode; and

a common electrode on the passivation layer.

19. The in-plane switching mode LCD device as claimed in claim 18, wherein the gate electrode includes a low resistance material.

20. The in-plane switching mode LCD device as claimed in claim 19, wherein the low resistance material includes one of aluminum (Al), copper (Cu), and silver (Ag).

21. The in-plane switching mode LCD device as claimed in claim 18, wherein the buffer layer includes a metal.

22. The in-plane switching mode LCD device as claimed in claim 21, wherein the buffer layer includes titanium (Ti).

23. The in-plane switching mode LCD device as claimed in claim 18, wherein the source and drain electrodes include a low resistance material.

24. The in-plane switching mode LCD device as claimed in claim 23, wherein the low resistance material includes one of aluminum (Al), copper (Cu), and silver (Ag).

25. The in-plane switching mode LCD device as claimed in claim 18, wherein the pixel electrode includes transparent conductive material.

26. The in-plane switching mode LCD device as claimed in claim 25, wherein the pixel electrode includes indium tin oxide.

27. The in-plane switching mode LCD device as claimed in claim 18, wherein the common electrode includes indium tin oxide.

28. A method for manufacturing an in-plane switching mode liquid crystal display (LCD) device comprising:

forming a gate electrode on a substrate;

forming a gate insulating film, a semiconductor layer, an ohmic contact layer, and a buffer layer on the gate electrode;

forming a pixel electrode on the buffer layer;

forming source and drain electrodes on the buffer layer;

forming a passivation layer on a surface of the substrate; and

forming a common electrode on the passivation layer.

29. The method as claimed in claim 28, wherein the gate electrode includes one of aluminum (Al), copper (Cu), and silver (Ag).

30. The method as claimed in claim 28, wherein the buffer layer includes titanium (Ti).

31. The method as claimed in claim 28, wherein the source and drain electrodes include one of aluminum (Al), copper (Cu), and silver (Ag).

32. The method as claimed in claim 28, wherein the pixel electrode includes indium tin oxide.

33. The method as claimed in claim 28, wherein the drain electrode is electrically connected with the pixel electrode.

34. The method as claimed in claim 28, wherein the common electrode includes indium tin oxide.

35. The method as claimed in claim 28, wherein the gate electrode is deposited by a sputtering process.

36. The method as claimed in claim 35, wherein the gate electrode is patterned using photolithography.

37. The method as claimed in claim 28, wherein the semiconductor layer, the ohmic contact layer, and the buffer layer are formed on the gate insulating film by a plasma enhanced chemical vapor deposition (PECVD) process.

38. The method as claimed in claim 37, wherein the semiconductor layer, the ohmic contact layer, and the buffer layer are patterned.

39. The method as claimed in claim 28, wherein the pixel electrode is formed by a sputtering process.

40. The method as claimed in claim 39, wherein the pixel electrode is patterned.

41. The method as claimed in claim 28, wherein the passivation layer is formed by a deposition process.